CLAIMS:

1. The electronic packaging structure, comprising a substrate (4); a first electrode layer (2) on a first side of said substrate (4); dielectric material (1) arranged in a preselected pattern on said first electrode layer (2); and a second electrode layer forming a plurality of second electrodes (3) which are arranged on said preselected pattern of dielectric material (1) to form a distributed capacitive structure together with said first electrode layer (2) as a first decoupling stage, characterized in that a second decoupling capacitor stage (9) is arranged on a second side of said substrate (4) opposite said first side and is electrically connected to said distributed capacitive structure, said second decoupling capacitor stage (9) having a capacity higher than that of said distributed capacitive structure.

2. The electronic packaging structure of claim 1, characterized in that said distributed capacitive structure consists of alternating polarities (5a, 5b) in a first direction on said substrate (4) and of alternating polarities (5a, 5b) in a second direction on said substrate (4) which is substantially perpendicular to said first direction.

3. The electronic packaging structure of claim 2, characterized in that contact areas (6) to said first electrode layer (2) are formed in apertures of said preselected patttern of said dielectric material (1) to provide one of said polarities of said distributed capacitive structure.

4. The electronic packaging structure of claim 1, characterized in that said substrate (4) comprises through holes (11) provided for connecting said distributed capacitive structure and said second decoupling stage (9).

5. The electronic packaging structure of claim 1, characterized in that said

high capacitance decoupling stage (9) consists of a plurality of capacitors.

6. The electronic packaging structure of claim 1, characterized in that the capacity of said second decoupling stage (9) is higher by a factor 5 to 100, preferably about 10, compared to the capacity of said distributed capacitive structure.

7. The electronic packaging structure of claim 1, characterized in that said substrate (4) is made of conductive material.

8. Integrated circuit, comprising a processor and an electronic packaging structure according to any of the preceding claims.

9. The integrated circuit of claim 7, wherein said second electrode layers (3) of the electronic packaging structure face said processor.